AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Original) A transistor comprising:

a first emitter for providing bipolar operation; and

a second emitter for providing ESD protection.

2. (Original) The transistor of claim 1, further including an ESD protection circuit coupled to the second emitter and further coupled to one of the group consisting of: a voltage pad, a ground, a ground plane, and a base of a transistor.

3. (Original) The transistor of claim 2, wherein the ESD protection circuit comprises at least one diode.

4. (Original) The transistor of claim 3, wherein each diode is selected from the group consisting of: a schottky diode, a Zener diode, a SiGe npn in diode connection, a varactor element, and a field effect transistor in diode configuration.

5. (Original) The transistor of claim 2, wherein the ESD protection circuit comprises at least one field effect transistor.

6. (Original) The transistor of claim 1, further including a circuit for disabling a current path for the first emitter during an ESD event.

7. (Original) The transistor of claim 6, wherein the disabling circuit includes a field effect transistor.

8. (Currently amended) A method of providing ESD protection comprising:

providing a transistor having a first emitter for providing bipolar operation and a second emitter; and

coupling the second emitter to an ESD protection circuit.

9. (Original) The method of claim 8, further comprising:

coupling the ESD protection circuit to a voltage pad;

disabling a current path from the second emitter to the voltage pad during normal operation; and

enabling the current path during an ESD event.

10. (Original) The method of claim 8, further comprising enabling a current path from the second emitter to a ground during an ESD event.

11. (Original) The method of claim 8, further comprising disabling a current path from the first emitter during an ESD event.

12. (Original) A differential circuit comprising:

a first transistor having a base coupled to a first voltage pad, a first emitter and a second emitter; and

a second transistor having a base coupled to a second voltage pad, a first emitter coupled to the first emitter of the first transistor, and a second emitter;

wherein the second emitter of the first transistor and the second emitter of the second transistor provide ESD protection.

13. (Original) The differential circuit of claim 12, wherein the second emitter of the first transistor is coupled to a first ESD protection circuit, and wherein the second emitter of the second transistor is coupled to a second ESD protection circuit.

14. (Original) The differential circuit of claim 13, wherein each ESD protection circuit is selected from the group consisting of: at least one diode, at least one varactor element, and at least one field effect transistor in diode configuration.

15. (Original) The differential circuit of claim 13, wherein the first ESD protection circuit is further coupled to the second voltage pad, and wherein the second ESD protection circuit is further coupled to the first voltage pad.

16. (Original) The differential circuit of claim 15, wherein each ESD protection circuit provides current flow in a forward bias mode of operation.

17. (Original) The differential circuit of claim 15, wherein the second emitter of the first transistor is further coupled to a field effect transistor that is further coupled to a ground.

18. (Original) The differential circuit of claim 17, wherein the field effect transistor is RC triggered based on a voltage at the first voltage pad.

19. (Original) The differential circuit of claim 12, wherein a current path from the first emitter of the first transistor is disabled during an ESD event, and wherein a current path from the first emitter of the second transistor is disabled during an ESD event.

20. (Original) The differential circuit of claim 19, wherein a first field effect transistor disables the current path from the first emitter of the first transistor, and wherein a second field effect transistor disables the current path from the first emitter of the second transistor.